What is claimed is:

1. A synchronization detection apparatus for detecting synchronization patterns arranged at specific bit intervals in a signal, comprising:

a comparison circuit for identifying data having the same number of bits as the synchronization pattern in order while shifting positions of data in the signal in units of bits and comparing the identified data with a predetermined synchronization pattern stored beforehand and

a synchronization processing circuit for establishing synchronization by using the identified data as the synchronization pattern when all results of comparisons with a predetermined number of the identified data arranged successively at said specific bit intervals are in agreement.

2. A synchronization detection apparatus as set forth in claim 1, wherein

said signal comprises a plurality of packets each having a specific bit length, and

said synchronization pattern is arranged at the head of a packet.

3. A synchronization detection apparatus for detecting synchronization patterns arranged at specific bit intervals in a signal, comprising:

a comparison circuit for identifying data having the same number of bits as the synchronization pattern in order while shifting positions of data in the signal in units of bits and comparing the identified data with a predetermined synchronization pattern stored beforehand;

a count circuit for adding or subtracting a predetermined value to or from an input first count to generate a second count when comparison results of said comparison circuit are in agreement;

a delay circuit for receiving as input the second count, delaying the same by a time corresponding to said specific bit intervals, and outputting the same as the first count; and

a synchronization processing state judging circuit for judging whether or not synchronization has been established based on the second count.

4. A synchronization detection apparatus as set forth in claim 3, wherein said comparison circuit

comprises a shift register comprising the same number of bits as said synchronization pattern and shifting said signal and

compares data stored in the shift register with a predetermined synchronization pattern stored beforehand.

5. A synchronization detection apparatus as set forth in claim 3, wherein

said delay circuit is an FIFO circuit having a bit length corresponding to said specific bit interval, and

said input second count is output as said first count in the order of input.

6. A synchronization detection apparatus as set forth in claim 3, wherein said count circuit sets an initial value as the second count when comparison results of said comparison circuit are not in agreement.

7. A synchronization detection apparatus as set forth in claim 3, wherein

said signal comprises a plurality of packets each having a specific bit length, and

said synchronization pattern is arranged at the head of said packet.

8. A receiving apparatus comprising a synchronization detection circuit for detecting synchronization patterns arranged at specific bit intervals in a received signal and generating a synchronization signal and a circuit for processing the received signal based on the synchronization signal,

wherein said synchronization detection circuit comprises:

a comparison circuit for identifying data having the same number of bits as the synchronization pattern in order while shifting positions of data in the received signal in units of bits and comparing the identified data with a predetermined synchronization pattern stored beforehand and

a synchronization processing circuit for generating said synchronization signal by using the identified data as the synchronization pattern when all results of said comparisons with a predetermined number of the identified data arranged successively at said specific bit intervals are in agreement.

9. A receiving apparatus comprising a synchronization detection circuit for detecting synchronization patterns arranged at specific bit intervals in a received signal and generating a synchronization signal and a circuit for processing the received signal based on the synchronization signal,

wherein said synchronization detection circuit comprises:

a comparison circuit for identifying data having the same number of bits as the synchronization pattern in order while shifting positions of data in the received signal in units of bits and comparing the identified data with a predetermined synchronization

pattern stored beforehand;

a count circuit for adding or subtracting a specific value to or from an input first count to generate a second count when results of said comparisons of said comparison circuit are in agreement;

a delay circuit for receiving as input the second count, delaying the same by a time corresponding to said specific bit interval, and outputting the same as the first count; and

a synchronization processing state judging circuit for judging whether or not synchronization has been established based on the second count.

10. A synchronization detection method for detecting synchronization patterns arranged at specific bit intervals in a signal, comprising the steps of:

identifying data having the same number of bits as the synchronization pattern in order while shifting positions of data in the signal in units of bits;

comparing the identified data with a predetermined synchronization pattern stored beforehand; and

using the identified data as the synchronization pattern and establishing synchronization when all results of comparisons with a predetermined number of the identified data arranged successively at

said specific bit intervals are in agreement.

11. A synchronization detection method for detecting a synchronization pattern arranged at specific bit intervals in a signal, comprising the steps of:

identifying data having the same number of bits as the synchronization pattern in order while shifting positions of data in the signal in units of bits;

comparing the identified data with a predetermined synchronization pattern stored beforehand;

adding or subtracting a specific value to or from a first count to generate a second count when comparison results of said comparison circuit are in agreement;

using the second count delayed by a time corresponding to said specific bit interval as the first count; and

judging whether or not synchronization has been established based on the second count.

12. A receiving method for detecting synchronization patterns arranged at specific bit intervals in a received signal, generating a synchronization signal, and processing the received signal based on the synchronization signal, comprising the steps of:

identifying data having the same number of bits

as the synchronization pattern in order while shifting positions of data in said received signal in units of bits;

comparing the identified data with a predetermined synchronization pattern stored beforehand; and

using the identified data as the synchronization pattern and generating said synchronization signal when all results of comparisons with a predetermined number of the identified data arranged successively at said specific bit intervals are in agreement.